WHAT IS CLAIMED IS:

1. A method of producing chip scale package, comprising:

attaching an array of two or more integrated circuit chips on a substrate;

dicing the array, attached to the substrate, into individual chip scale packages, each chip scale package comprising only one integrated circuit chip.

2. The method according to claim 1, wherein each of the two or more integrated circuit chips comprises:

a plurality of bond pads aligned in a single row and centrally disposed on an upper surface of the integrated circuit chip, and

a plurality of conductive bumps formed on the plurality of bond pads.

3. A method of producing a chip scale package, comprising:

providing a wafer, the wafer comprising a plurality of integrated circuit chips;

dicing the wafer into a plurality of chip arrays, each array comprising two or more integrated circuit chips;

attaching each chip array on a substrate;

dicing each array, attached to the substrate, into individual chip scale packages, each individual chip scale package comprising only one integrated circuit chip.

4. The method according to claim 3, wherein each chip array comprises one of a 2 x 2 matrix, a 3 x 3 matrix, or a 4 x 4 matrix of integrated circuit chips.

5. A method of producing a chip scale package, comprising:

providing a wafer, the wafer comprising a plurality of integrated circuit chips, each integrated circuit chip comprising

a plurality of bond pads aligned on an upper surface of the integrated circuit chip and

a plurality of conductive bumps formed on the plurality of bond pads;

dicing the wafer into a plurality of chip arrays, each array comprising two or more integrated circuit chips;

mounting each array on a substrate such that the bumps align with corresponding solder pad openings on an upper surface of the substrate;

reflowing the integrated circuit chips of each array, thereby melting the bumps and establishing a conductive joint between the integrated circuit chips and the substrate;

under fill encapsulating the integrated circuit chips and the substrate; and

dicing the array, joined to the substrate, into individual chip scale packages, each comprising only one integrated circuit chip.

6. The method according to claim 5, further comprising:

prior to mounting each array on a substrate, dipping each array in flux material, such that flux material adheres to the bumps;

wherein, when each array is mounted on a substrate, the flux material adheres the bumps to the solder pad openings.

7. The method according to claim 6, further comprising:

after reflowing the integrated circuit chips, cleaning the integrated circuit chips, the bumps, and the substrate to remove flux material.

8. The method according to claim 5, wherein:

under fill encapsulating the integrated circuit chips comprises injecting encapsulation material into a gap between the integrated circuit chips and the substrate.

9. The method according to claim 5, further comprising:

before dicing the array into individual chip scale packages, forming solder balls, conductively connected to the bumps, on the under surface of the substrate.

10. A multi-chip array package, comprising:

a substrate; and

a chip array, comprising two or more integrated circuit chips, flip-chip mounted on the substrate.

11. The multi-chip array package according to claim 10, wherein:

each of the two or more integrated circuit chips comprises a plurality of conductive bumps formed on an upper surface thereof; and

the chip array is mounted on the substrate such that the upper surface the two or more integrated circuit chips faces the substrate and the plurality of conductive bumps are conductively coupled to the substrate.

12. The multi-chip array package according to claim 11, further comprising:

encapsulation material disposed between the chip array and the substrate and around the plurality of conductive bumps.